NARAYANA ENGINEERING COLLEGE
NELLORE(AUTONOMOUS)

APPROVED BY AICTE AND PCI NEW DELHI AND AFFILIATED TO JNTUA ANANTAPURAMU
A PART OF NARAYANA GROUPEDUCATIONAL OF INSTITUTIONS, INDIA.

Department of Electronics & Communication Engineering

1	Name of the Activity/Event	Expert Lecture on **"Verilog HDL"**		
2	Date of Activity/Event	**22-11-2023**		
3	Organized by	**Department of Electronics And Communication Engineering**		
4	Place of Activity/event	Visvesvaraya Auditorium		
5	Resource persons / guest / organization	**M. Madana Gopal** Star VLSI Services pvt. Ltd., Banglore		
6	Type of activity/Event	Expert Lecture		
7	Activity/Event objectives	1. This course aims at providing an opportunity for students to enrich their knowledge and skill in developing various solutions for solving engineering problems in the society. 2. This program serves as a platform for students to work with recent trends in Electronic simulation related areas.		
8	Participation	Students	Faculty	Total Participation
		204	-	204
9	General remarks	1. Introduction to Verilog. 2. Study of HDL.		
10	Suggested Improvements	-		
11	Enclosures	1. Program report with Snapshots 2. Attendance sheet		
12	Signature of Co-ordinator			

A Guest lecture was conducted by the Department of Electronics and **C**ommunication **E**ngineering, NEC Nellore on **22 November 2023.** Resource person M. Madana Gopal, Star VLSI Services Pvt. Ltd., Banglore, has taken a lecture on topic **Verilog HDL(IC Applications)** for 3rd B.Tech students in C Block Main Auditorium. Total of around 204 students and staff participate in this programme.

Presentation on Verilog HDL

Speaker explains the Basics of Lexical convention and Data types

Lexical conventions: Lexical conventions in Verilog are similar to the C programming language. Verilog language source text files are a stream of lexical tokens. A lexical token may consist of one or more characters, and every single character is in exactly one token. The tokens can be keywords, comments, numbers, white space, or strings.

Resource person sharing information regarding in this session

In the next session subject expert discussed on the concepts Systems tasks and compiler directives. Discussion continued by covering the topics **Modules and Ports:** Module definition, port declaration, connecting ports, Hierarchical names. Session ended by sharing the information regarding **Modeling:**

Gate level modeling, data flow modeling, Behavioral modeling.

Students and Staff participated in programme

Resource person discussed with real time examples and the session was made really interactive by providing an opportunity to suggest a solution to real life scenario with the help of images and videos.